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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

WU, DOROTHY

ART UNIT	PAPER NUMBER
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2697

DATE MAILED: 03/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/265,819

Applicant(s)

SHINOHARA, MAHITO

Examiner

Dorothy Wu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 March 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6, 7.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

✓ 1. The drawings are objected to because Figs. 3 and 4 do not adequately demonstrate how output line 10 connects to switches 9 and 14.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 9-1, 9-2 in Fig. 3, and 2 in Fig. 4 (on page 10, lines 22-23).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: the disclosure repeatedly mentions parts of the invention without their reference characters. Some examples include, on page 7, "preliminary operation mode generation circuit" on lines 13-14, "reference clock generation circuit" on lines 14-15, and "drive pulse generation circuit" on lines 16-17. All subsequent occurrences should also be noted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5, 6, 7, 8, 10, 11, 12, 14, and 16 are rejected under 35 U.S.C 112, second paragraph.

Claims 5, 6, 7, 8, 11, 12 all recite the limitation "drive mode control clock signal." There is insufficient antecedent basis in the disclosure for this limitation in the claim.

Claim 5 recites the limitation "drive pulse generation circuit" in lines 4-5 of page 14. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "said state image pickup chip" in line 14 of page 16. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitations "semiconductor chip" in line 20, page 16, "basic clock generation circuit" on line 22, "reference pulse generation circuit chip" on line 23, and "semiconductor chip" on lines 26-27. There is insufficient antecedent basis for any of these limitations in the claim.

Claim 12 recites the limitation "preliminary operation control clock signal" and "preliminary operation control circuit" on line 7, page 17. Claim 12 also recites the limitation "said chip" twice in line 14, page 17. There is insufficient antecedent basis for any of these limitations in the claim.

Claim 14 recites the limitation "switch is adapted to turn off the power supply to said first or second control circuit" in lines 10-12, on page 18. There is insufficient antecedent basis for

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this limitation in the claim. The specification does not teach that the first control circuit is ever turned off.

Claim 16 recites the limitation "signal processing circuit is controlled by said second control circuit" in lines 24-25, page 18. There is insufficient antecedent basis for this limitation in the claim. The specification teaches that the microprocessor itself executes signal processing, but does not teach that the microprocessor controls a signal processor (page 8, lines 12-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Halvis et al, U.S. Patent 5,164,832.

Regarding claim 1, the admitted prior art teaches a solid state image pickup device comprising an image pickup unit and a drive timing control device that outputs a clock signal to determine the timing of the drive pulse of the image sensor, which reads on the reference clock generation circuit (page 1, lines 8-15, and Fig. 1). The admitted prior art does not teach a plurality of photoelectric conversion elements, nor does it teach that the image pickup unit and reference clock generation circuit are formed on the same semiconductor chip. Halvis et al teaches a solid-state image sensing device with a plurality of photosensitive image detector elements (col. 1, lines 10-12). Halvis et al also teaches that the readout circuitry and

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photoelectric conversion elements may be formed on the same semiconductor substrate (col. 1, lines 45-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the solid state image pickup device taught by the admitted prior art with the practice of forming functional units on the same semiconductor chip taught by Halvis et al to make an apparatus with the parts of the admitted prior art formed on the same chip. One of ordinary skill would have been motivated to make such a modification because manufacturing parts on a single chip results in lower area.

Regarding claim 2, the admitted prior art teaches a drive pulse generation circuit for driving the image pickup unit, wherein the drive pulse generation circuit is formed on the same semiconductor chip as the image pickup unit (Fig. 1).

Regarding claim 9, the admitted prior art teaches a solid state image pickup device with a solid state image pickup chip including an image pickup unit and a drive pulse generation circuit chip including a drive pulse generation circuit for driving the image pickup unit (Fig. 2). The admitted prior art also teaches a drive timing control device that outputs a clock signal to determine the timing of the drive pulse of the image sensor, which reads on the reference clock generation circuit (page 1, lines 8-15). The admitted prior art does not teach that the reference clock generation circuit is formed on the drive pulse generation circuit chip. Halvis et al teaches that the readout circuitry may be integrated on a separate substrate from the photoelectric conversion elements (col. 1, lines 48-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the solid state image pickup device taught by the admitted prior art with the practice of forming readout circuitry and photoelectric conversion elements on separate semiconductor substrates taught by Halvis et al to

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make an apparatus with the parts of the admitted prior art wherein the readout circuitry is monolithically formed on a separate chip from the photoelectric conversion elements. One of ordinary skill would have been motivated to make such a modification because forming readout circuitry on a separate chip results in a hybrid image sensing apparatus.

5. Claims 3, 4, 10, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Halvis et al, U.S. Patent 5,164,832, and further in view of Yasuda, U.S. Patent 6,130,710.

Regarding claims 3 and 4, the admitted prior art in view of Halvis et al teach the apparatus according to the limitations of claims 1 and 2. See above. Halvis et al teaches that the readout circuitry and photoelectric conversion elements may be formed on the same semiconductor substrate (col. 1, lines 45-48). The admitted prior art in view of Halvis et al do not teach a preliminary control circuit for driving the image pickup unit in a predetermined operation mode. Yasuda teaches a first synchronizing signal generator operable at a video rate for low resolution, which reads on the preliminary control circuit, for driving the imager (col. 4, lines 3-5, and Fig. 1). Yasuda also teaches a first image pickup mode that operates at a low, video rate, which reads on the predetermined preliminary operation mode (col. 2, lines 12-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by the admitted prior art in view of Halvis et al with the preliminary control circuit taught by Yasuda to make an image sensing device with a preliminary control circuit that enables the image sensing device to operate in a preliminary, low resolution mode, wherein the image sensing device and control circuits are formed on the

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same semiconductor substrate. One of ordinary skill would have been motivated to make such a modification because operating the image sensing device in a low resolution facilitates the capture of images in real time, and forming circuits on the same substrate results in less area.

As best understood from the language of the claims, regarding claim 10, the admitted prior art in view of Halvis et al teach the apparatus according to the limitations of claims 9. See above. Halvis et al teaches that the readout circuitry may be integrated on a separate substrate from the photoelectric conversion elements (col. 1, lines 48-51). The admitted prior art in view of Halvis et al do not teach a preliminary control circuit for driving the image pickup unit in a predetermined operation mode. Yasuda teaches a first synchronizing signal generator operable at a video rate for low resolution, which reads on the preliminary control circuit, for driving the imager (col. 4, lines 3-5, and Fig. 1). Yasuda also teaches a first image pickup mode that operates at a video rate, which reads on the predetermined preliminary operation mode (col. 2, lines 12-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by the admitted prior art in view of Halvis et al with the preliminary control circuit taught by Yasuda to make an image sensing device with a preliminary control circuit that enables the image sensing device to operate in a preliminary, low resolution mode, wherein the image sensing device and control circuits are formed on separate semiconductor substrates. One of ordinary skill would have been motivated to make such a modification because operating the image sensing device in a low resolution facilitates the capture of images in real time, and forming circuits on separate substrates results in a hybrid image sensing apparatus.

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As best understood from the language of the claim, regarding claim 13, the admitted prior art teaches a solid state image pickup device comprising an image pickup unit, a drive pulse generation circuit for driving the image pickup unit, and a drive timing control device that outputs a clock signal to determine the timing of the drive pulse of the image sensor, which reads on the reference clock generation circuit (page 1, lines 11-16, and Fig. 1). The admitted prior art does not teach a plurality of photoelectric conversion elements. Halvis et al teaches a solid-state image sensing device with a plurality of photosensitive image detector elements (col. 1, lines 10-12). The admitted prior art does not teach first and second controls for controlling the operation mode of the drive pulse generation circuit, nor does the admitted prior art teach a switch for connecting the first or second control circuit to the drive pulse generation circuit. Yasuda teaches first and second synchronizing signal generators, which read on the first and second control circuits, for controlling the operation mode of a timing generator that drives the image pickup unit (col. 4, lines 3-9). Yasuda also teaches a switch for connecting the first or second synchronizing signal generator to the timing generator (col. 4, lines 6-7, and Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the image pickup unit, drive pulse generation circuit, and reference pulse generation circuit taught by the admitted prior art with the plurality of photoelectric conversion elements taught by Halvis et al with the first and second control circuits and switch taught by Yasuda to make an image sensing apparatus with a plurality of driving modes. One of ordinary skill would have been motivated to make such a modification because the plurality of driving modes results in greater control over image quality and image processing speeds.

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Regarding claim 15, Yasuda teaches that the driving signals from the first and second synchronizing signal generators have different frequencies (col. 4, lines 30-34). Yasuda also teaches that a possible method for implementing the low resolution mode controlled by the first synchronizing signal generator is to partially read out a specific area of the image sensor (col. 4, lines 3-5, 49-54). It would have been obvious to one of ordinary skill that reading out a partial area of an image sensor results in a lower frequency driving signal and thus consumes less power than reading out the entire image sensor. Therefore, the first control circuit functions with a lower power consumption than the second control circuit.

As best understood from the language of the claim, regarding claim 16, Yasuda teaches a second color processing section for executing image processing on the signal from the image pickup unit, wherein the second color processing section is controlled by the second synchronizing signal generator (col. 3, lines 59-60; col. 4, lines 5-6; and Fig. 1).

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Halvis et al, U.S. Patent 5,164,832, in view of Yasuda, U.S. Patent 6,130,710, and further in view of Hyncek et al, U.S. Patent 5,278,656.

As best understood from the language of the claim, the admitted prior art in view of Halvis et al in view of Yasuda teach the apparatus with the limitations of claim 13. See above. The admitted prior art in view of Halvis et al in view of Yasuda do not teach that the switch is adapted to turn off the power supply to the first or second control circuit which is not connected to the drive pulse generation circuit. Hyncek et al teaches the turning off of a functional unit when it is not in use to conserve power (col. 7, lines 23-28). Therefore, it would have been

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obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus of the admitted prior art in view of Halvis et al in view of Yasuda with the practice of turning off functional units when they are not in use taught by Hyncek et al to make a switch that turns off the power supply to the control circuit that is not connected to the drive pulse generation circuit. One of ordinary skill would have been motivated to make such a modification to produce a solid state image pickup device with less power consumption.

7. Claims 5-8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Halvis et al, U.S. Patent 5,164,832, in view of Yasuda, U.S. Patent 6,130,710, and further in view of Roberts et al, U.S. Patent 5,576,757.

As best understood from the language of the claims, regarding claims 5 and 6, the admitted prior art in view of Halvis et al in view of Yasuda teach the apparatus according to the limitations of claims 3 and 4. See above. The admitted prior art teaches the supply of drive mode control signals and a reference clock signal to the drive pulse generation circuit for driving the image pickup unit (page 1, lines 14-15, and Fig. 1). Yasuda teaches a switch for multiplexing drive signals from a plurality of synchronizing signal generators (col. 4, lines 3-7, and Fig. 1). Halvis et al teaches that the readout circuitry and photoelectric conversion elements may be formed on the same semiconductor substrate (col. 1, lines 45-48), thereby teaching that the switch may be formed on the same semiconductor chip. The admitted prior art teaches that the driving signals may come from the exterior of the semiconductor chip (Fig. 1). Halvis et al teaches that the readout circuitry and photoelectric conversion elements may be formed on the

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same semiconductor substrate (col. 1, lines 45-48), thereby teaching that driving signals may come from the interior of the semiconductor chip as well.

The admitted prior art in view of Halvis et al in view of Yasuda do not teach that a drive mode control signal comes from a preliminary control circuit or that a reference clock signal comes from a reference clock generation circuit. Roberts et al teaches a reference clock signal from a digital control unit 9, which reads on the reference clock generation circuit (col. 4, lines 15-17, and Fig. 1). Roberts et al also teaches a drive mode control signal that comes from operator variable control switches, which reads on the preliminary control circuit (col. 5, lines 10-34, and Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the practice of using drive mode control signals and a reference clock signal for determining the timing of the drive pulse generation circuit, the supply of driving signals from either the interior or exterior of the semiconductor chip, the plurality of control circuits supplying drive signals, and the switch for multiplexing between the driving signals supplied by the plurality of control circuits taught by the admitted prior art in view of Halvis et al in view of Yasuda, with the practice of having separate circuits generate the clock and drive mode control signals taught by Roberts et al to make an image pickup device comprising a switch for selectively supplying the drive pulse generation circuit with a drive mode control signal and a reference clock signal, wherein the drive mode control signal and reference clock signal may come from the preliminary control circuit and reference clock generation circuit from the interior of the semiconductor chip, or from the exterior of the chip, and the wherein the switch is part of the readout circuitry and is thus formed on the semiconductor substrate. One of

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ordinary skill would have been motivated to make such a modification because switching between different driving signals results in a plurality of driving modes for the image sensor, and the supply of driving signals from the exterior of the chip results in a hybrid image sensing apparatus.

As best understood from the language of the claims, regarding claims 7 and 8, the admitted prior art in view of Halvis in view of Yasuda teach the apparatus with the limitations of claims 5 and 6. See above. The admitted prior art teaches the use of drive mode control signals and a reference clock signal to control the driving of the image sensor (page 1, lines 14-15). Yasuda teaches two operation modes wherein the solid state image pickup device operates at a low, video rate in the first mode and a high resolution rate in the second mode (col. 2, lines 12-15). Yasuda also teaches a first synchronizing signal generator for low resolution corresponding to the first mode, a second synchronizing signal generator for high resolution corresponding to the second mode, and a switch for selecting which synchronizing signal generator's signals will drive the image pickup device (col. 4, lines 3-7, and Fig. 1). The admitted prior art teaches that driving signals may come from the exterior of the chip (Fig. 1). Halvis et al teaches that the readout circuitry and photoelectric conversion elements may be formed on the same semiconductor substrate (col. 1, lines 45-48), thereby teaching that driving signals may come from the interior of the semiconductor chip as well. Yasuda further teaches that the driving signals from the first and second synchronizing signal generators have different frequencies (col. 4, lines 30-34). Yasuda also teaches that a possible method for implementing the low resolution mode is to partially read out only a specific area of the image sensor (col. 4, lines 49-54). It would have been obvious to one of ordinary skill that reading out a partial area of an image

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sensor results in a lower frequency driving signal and thus consumes less power than reading out the entire image sensor.

The admitted prior art in view of Halvis et al in view of Yasuda do not teach synchronization of the image pickup unit with the reference clock signal and preliminary operation control signal from the reference clock generation circuit and preliminary operation control circuit, respectively. Roberts et al teaches a reference clock signal from a digital control unit 9, which reads on the reference clock generation circuit (col. 4, lines 15-17, and Fig. 1). Roberts et al also teaches a drive mode control signal that comes from operator variable control switches, which reads on the preliminary control circuit (col. 5, lines 10-34, and Fig. 1). Thus, Roberts et al teaches that the driving and clock signals may come from separate circuits.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the provision of clock and driving signals, the low and high resolution modes, the synchronization of the image pickup unit with driving signals in accordance with the operation mode, the option of having the driving signals come from the interior or exterior of the semiconductor chip, taught by the admitted prior art in view of Halvis et al in view of Yasuda, with the practice of supplying driving and clock signals from separate circuits taught by Roberts et al to make an image sensing apparatus that synchronizes the image pickup unit with clock and driving signals in accordance with the operation mode, wherein the clock and driving signals may come from the interior or exterior of the semiconductor chip, wherein the operation of the semiconductor chip is executed with a lower power consumption in the low resolution mode than in the high resolution mode. One of ordinary skill would have been motivated to make such a modification because providing a plurality of driving modes results in

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greater control over image quality, and the supply of driving signals from the exterior of the chip results in a hybrid image sensing apparatus.

As best understood from the language of the claims, regarding claim 11, the admitted prior art in view of Halvis et al in view of Yasuda teach the apparatus according to the limitations of claim 10. See above. The admitted prior art teaches the supply of drive mode control signals and a reference clock signal to the drive pulse generation circuit for driving the image pickup unit (page 1, lines 14-15, and Fig. 1). Yasuda teaches a switch for multiplexing drive signals from a plurality of synchronizing signal generators (col. 4, lines 3-7, and Fig. 1). Halvis et al teaches that the readout circuitry may be integrated on a substrate separate from the photoelectric conversion elements (col. 1, lines 48-51), and the switch for multiplexing driving signals is part of the readout circuitry. The admitted prior art teaches that the driving signals may come from the exterior of the semiconductor chip (Fig. 1). Halvis et al teaches that the readout circuitry may be integrated on a substrate separate from the photoelectric conversion elements (col. 1, lines 45-48), thereby teaching that driving signals may come from the interior of the drive pulse generation circuit chip as well.

The admitted prior art in view of Halvis et al in view of Yasuda do not teach that a drive mode control signal comes from a preliminary control circuit or that a reference clock signal comes from a reference clock generation circuit. Roberts et al teaches a reference clock signal from a digital control unit 9, which reads on the reference clock generation circuit (col. 4, lines 15-17, and Fig. 1). Roberts et al also teaches a drive mode control signal that comes from operator variable control switches, which reads on the preliminary control circuit (col. 5, lines 10-34, and Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the practice of using drive mode control signals and a reference clock signal for determining the timing of the drive pulse generation circuit, the supply of driving signals from either the interior or exterior of the semiconductor chip, the plurality of control circuits supplying drive signals, and the switch for multiplexing between the driving signals supplied by the plurality of control circuits formed on the drive pulse generation circuit chip taught by the admitted prior art in view of Halvis et al in view of Yasuda, with the practice of having separate circuits generate the clock and drive mode control signals taught by Roberts et al to make an image pickup device comprising a switch for selectively supplying the drive pulse generation circuit with a drive mode control signal and a reference clock signal, wherein the drive mode control signal and reference clock signal may come from the preliminary control circuit and reference clock generation circuit from the interior of the semiconductor chip, or from the exterior of the chip, and the wherein the switch is part of the readout circuitry and is thus formed on a separate semiconductor substrate from the photoelectric conversion elements. One of ordinary skill would have been motivated to make such a modification because switching between different driving signals results in a plurality of driving modes for the image sensor, and the supply of driving signals from the exterior of the chip results in a hybrid image sensing apparatus.

As best understood from the language of the claims, regarding claim 12, the admitted prior art in view of Halvis in view of Yasuda teach the apparatus with the limitations of claim 11. See above. The admitted prior art teaches the use of drive mode control signals and a reference clock signal to control the driving of the image sensor (page 1, lines 14-15). Yasuda teaches two

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operation modes wherein the solid state image pickup device operates at a low, video rate in the first mode and a high resolution rate in the second mode (col. 2, lines 12-15). Yasuda also teaches a first synchronizing signal generator for low resolution corresponding to the first mode, a second synchronizing signal generator for high resolution corresponding to the second mode, and a switch for selecting which synchronizing signal generator's signals will drive the image pickup device (col. 4, lines 3-7, and Fig. 1). Halvis et al teaches that the readout circuitry may be integrated on a substrate separate from the photoelectric conversion elements (col. 1, lines 48-51), and the switch for multiplexing driving signals is part of the readout circuitry. The admitted prior art teaches that driving signals may come from the exterior of the chip (Fig. 1). Halvis et al teaches that the readout circuitry may be integrated on a substrate separate from the photoelectric conversion elements (col. 1, lines 45-48), thereby teaching that driving signals may come from the interior of the drive pulse generation circuit chip as well. Yasuda further teaches that the driving signals from the first and second synchronizing signal generators have different frequencies (col. 4, lines 30-34). Yasuda also teaches that a possible method for implementing the low resolution mode is to partially read out only a specific area of the image sensor (col. 4, lines 49-54). It would have been obvious to one of ordinary skill that reading out a partial area of an image sensor results in a lower frequency driving signal and thus consumes less power than reading out the entire image sensor.

The admitted prior art in view of Halvis et al in view of Yasuda do not teach synchronization of the image pickup unit with the reference clock signal and preliminary operation control signal from the reference clock generation circuit and preliminary operation control circuit, respectively. Roberts et al teaches a reference clock signal from a digital control

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unit 9, which reads on the reference clock generation circuit (col. 4, lines 15-17, and Fig. 1).

Roberts et al also teaches a drive mode control signal that comes from operator variable control switches, which reads on the preliminary control circuit (col. 5, lines 10-34, and Fig. 1). Thus, Roberts et al teaches that the driving and clock signals may come from separate circuits.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the provision of clock and driving signals, the low and high resolution modes, the synchronization of the image pickup unit with driving signals in accordance with the operation mode, the option of having the driving signals come from the interior or exterior of the semiconductor chip, taught by the admitted prior art in view of Halvis et al in view of Yasuda, with the practice of supplying driving and clock signals from separate circuits taught by Roberts et al to make an image sensing apparatus that synchronizes the image pickup unit with clock and driving signals in accordance with the operation mode, wherein the clock and driving signals may come from the interior or exterior of the semiconductor chip, wherein the operation of the semiconductor chip is executed with a lower power consumption in the low resolution mode than in the high resolution mode. One of ordinary skill would have been motivated to make such a modification because providing a plurality of driving modes results in greater control over image quality, and the supply of driving signals from the exterior of the chip results in a hybrid image sensing apparatus.

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Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ohzu et al, U.S. Pub. 2002/0167601 A1, teaches that the photoelectric conversion elements and readout apparatus may be integrated on the same chip.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dorothy Wu whose telephone number is 703-305-8412. The examiner can normally be reached on Monday-Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Williams can be reached at 703-305-4863.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC 20231

Or faxed to:

703-872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377

Dwight Wm

DW
March 10, 2003

Kimberly A. Williams
Kimberly A. Williams
Primary Examiner
Technology Center 2600

KA Williams
Kimberly A. Williams
Primary Examiner
Technology Center 2600